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Optoelectronic performance, absorber structure and composition for optimum absorbers

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Partners	IREC, NU and UU-ASC
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1 General introduction

Four synthesis routes have been considered in WP2 and of these three were vacuum based processes based on magnetron sputter deposition of precursor layers followed by subsequent a reactive anneal/conversion step to form the absorber layer. These routes include the two-stage process (deposition of metallic multilayers followed by heating with elemental selenium to form CZTSe) developed at NU. A process based on the sputter deposition of thick metallic layers and conversion to CZTSSe at IREC and reactive co-sputtering of both metal Zn and Sn and CuS followed by a reactive anneal developed at UU/ASC. All synthesis routes yielded devices with efficiencies of ~8 %. The incorporation of Ge in the IREC process yielded a device with over 10.4 % conversion efficiency. IREC also investigated a non-vacuum deposition route – spray pyrolysis. Whilst the results were not promising for that particular process at IREC and work was terminated, an alternative non-vacuum process at EMPA in WP4 yielded devices with over 11 % conversion efficiency. In addition to the development of absorber layers, improvement and optimisation of interfaces at IREC contributed to device improvements.

Therefore, it is proposed that the processes identified above should be considered as viable synthesis routes that yield device-quality absorber layers. Each has the potential to achieve high performance devices and pursuing multiple routes enables a greater understanding of the relationship between synthesis and properties than could be achieved by considering only one route.

2. Partner: NU - Development of CZTSe based absorbers by PVD processes

The initial optimisation of synthesis process used by Northumbria resulted in CZTSe absorber layers that yielded device conversion efficiencies of 8.1% (AM1.5, 1000 Wm^{-2}, 25 °C) with significant potential for further optimisation. The properties of the resulting absorber layers were influenced by the detail of conversion conditions. Notwithstanding this, the performances reported were produced when absorbers were synthesised using both RTP and conventional tube furnace (slow heating) indicating that it is a relatively tolerant process and it will be developed further. The synthesis route involved a 2-stage process as a (as described in detail in Milestone 2.2, the first stage involves the sputter deposition of a mixed Cu, Zn and Sn precursor layer from high-purity elemental targets. The second stage involves conversion to the selenide by heating the precursors inside a graphite box with an excess of elemental selenium, using a temperature of 500 °C and a 15 minute dwell time.

Cross-section SEM images for the samples before and after the RTP selenisation step can be seen in Figure 1. The process yielded device efficiencies of 8.1%, produced using non-stoichiometric absorbers and without an AR coating. The J-V characteristics of the best solar cell synthesised with this process can be seen in Figure 2.

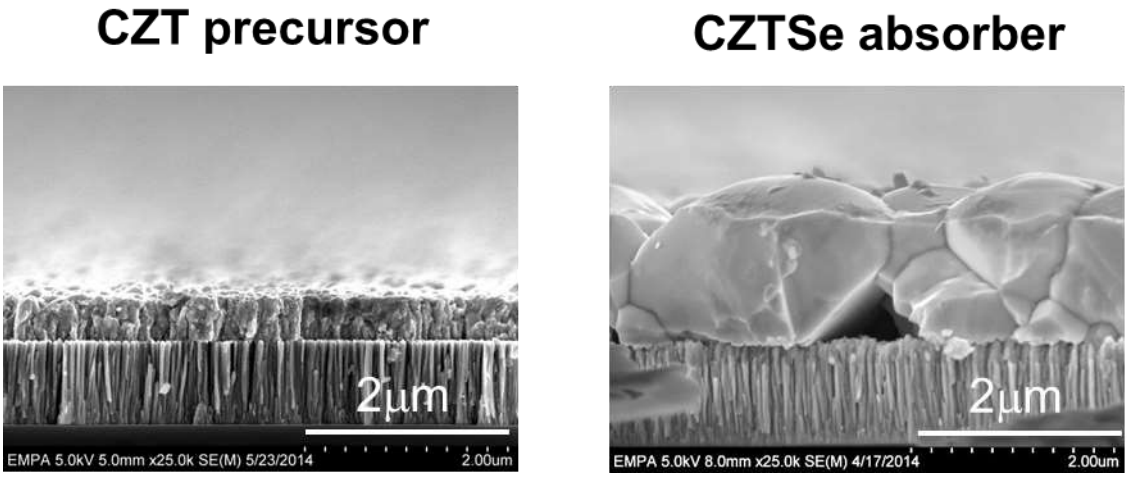

Figure 1. Cross sectional image of the Cu-Zn-Sn precursor and the $Cu_2ZnSnSe_4$ absorber layer.

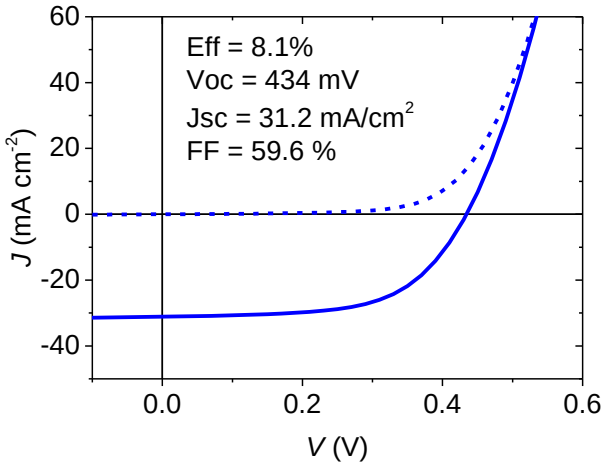

Figure 2. Dark and illuminated J-V characteristics of the solar cell developed at NU

Influence of composition

In the kesterite community, it is well established that higher efficiency solar cells based on CZT(S,Se) are produced with absorbers with Cu-poor (Cu/Zn+Sn<1) and Zn-rich (Zn/Sn>1) compositions[1]. At NU the influence of the Cu content within this compositional range was studied with the most optimised processing conditions. A set of samples with different compositions, were produced using the same selenisation process (detailed in Table 2.1).

Table 1. Sample composition table: Atomic metal ratios for the Cu-Zn-Sn and CZTSe absorber layers of the study presented. The technique used for measuring the composition is specified at the top of each column. Data from reference 2.

	[XRF-Precursors]		[XRF-CZTSe]		[EDX-CZTSe]	
Sample	**Cu/(Zn+Sn)**	**(Zn/Sn)**	**Cu/(Zn+Sn)**	**(Zn/Sn)**	**Cu/(Zn+Sn)**	**(Zn/Sn)**
Sample 1	0.90	1.03	0.99	1.04	0.86	1.00
Sample 2	0.70	1.09	0.80	1.18	0.75	1.17
Sample 3	0.65	1.12	0.72	1.28	0.66	1.24

The current density-voltage (J-V) characteristics of the solar cells prepared with the three set of samples were analysed and a summary is shown in Figure 3. It was concluded that the samples with the least Cu content were the most efficient due to an increase of the open circuit voltage of the solar cells as they become more Cu deficient.

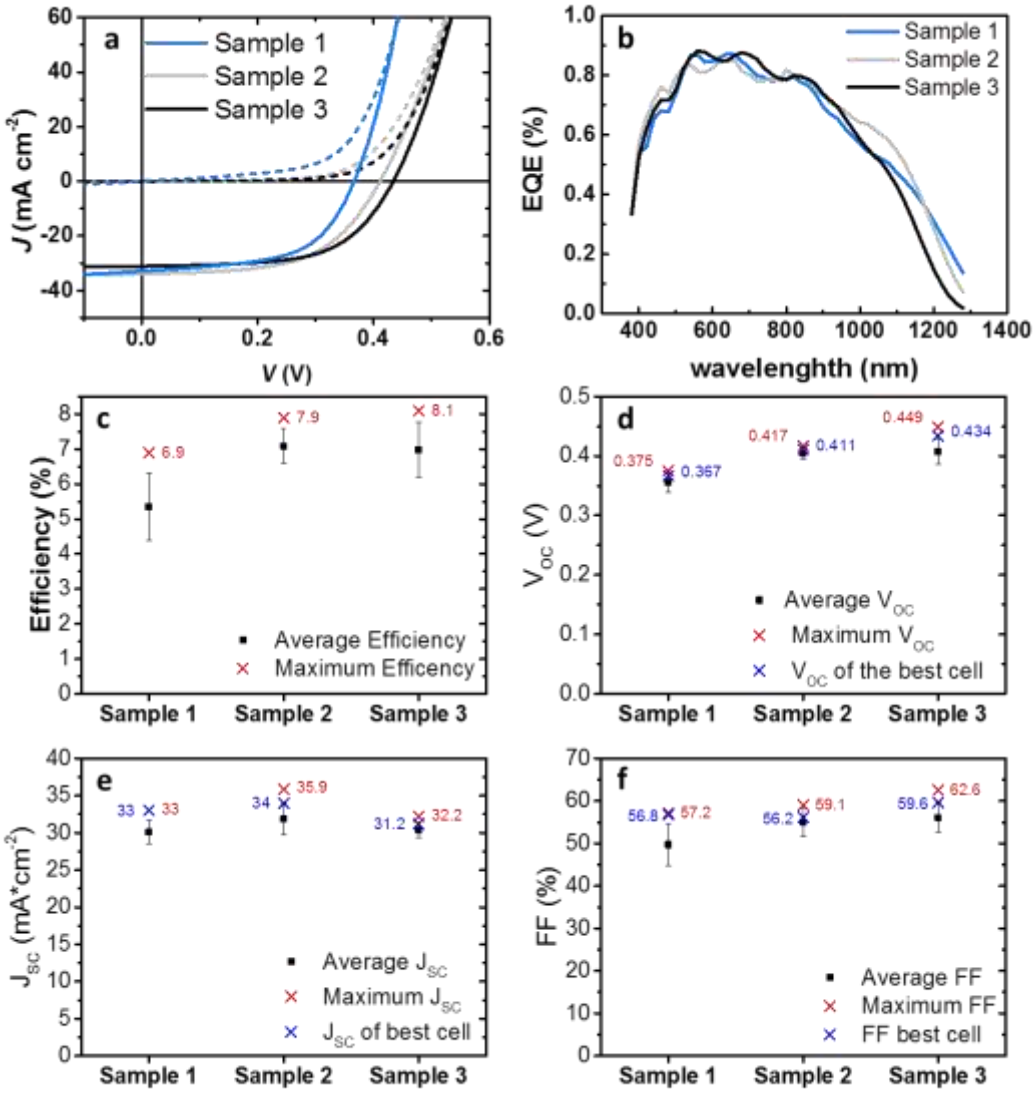

Figure 3. a) Current density – voltage (JV) curves and b) EQE of the best solar cells of each sample of this study. c), d), e), and f) show a summary of the average and standard deviation of the main optoelectronic parameters for the different devices (based on an average of 9 representative cells from each sample). Maximum values and the values for the best cells (highest efficiency) of each sample are also represented. Data from [2].

Future synthesis routes

Future synthesis routes at Northumbria will consider an optimisation of the selenisation step, exploring the influence and correlation of the time and temperature parameters of this process. The goal will be reducing the processing time of the selenisation process without compromising the performance of the devices produced.

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Partner UU/ASC

The synthesis route adopted at UU-ASC is based on the 2-stage process, i.e. reactive co-sputtering of CuS-Zn-Sn targets followed by rapid thermal annealing in a sulphur excess atmosphere. Reactive co-sputtering process allows the uniform intermix of Cu-Zn-Sn-S elements into a precursor film with controlled composition. At UU-ASC, such deposition was performed in an H_2S gas reactive sputtering system (Von Ardenne CS600) with a three-target configuration [3, 4]. Optimized deposition rate in the system so far was obtained using a constant sputtering pressure of 0.7 Pa resulting from the supply of 1:1 H_2S: Ar gases with 30 sccm total flow rate, as well as the controlled power on the targets. The substrate holder temperature was kept at about 180 °C during the deposition to eliminate the delamination and crack issues of the annealed film in a later step [3]. As the last stage for absorber formation, annealing process has been demonstrated to be crucial for high performance solar cells by improving material quality. The precursor films were annealed in a tube furnace at UU-ASC [5]. In this system, a fast ramping (cooling) thermal process can be realized by transferring the samples from a cold zone into a hot zone, and vice versa. The baseline annealing process is composed of a heat treatment at 560 °C for 10 min under a static Ar atmosphere (35 kPa). The as sputtered films were loaded into a closed graphite box of 5×5 cm^2 size along with elemental sulphur excess. Typical Raman spectra of the as sputtered and annealed CZTS film are shown in Figure 4(a). A great sharpening of the CZTS peak of the annealed film implies high CZTS absorber quality, pointing to the essentiality of the annealing process.

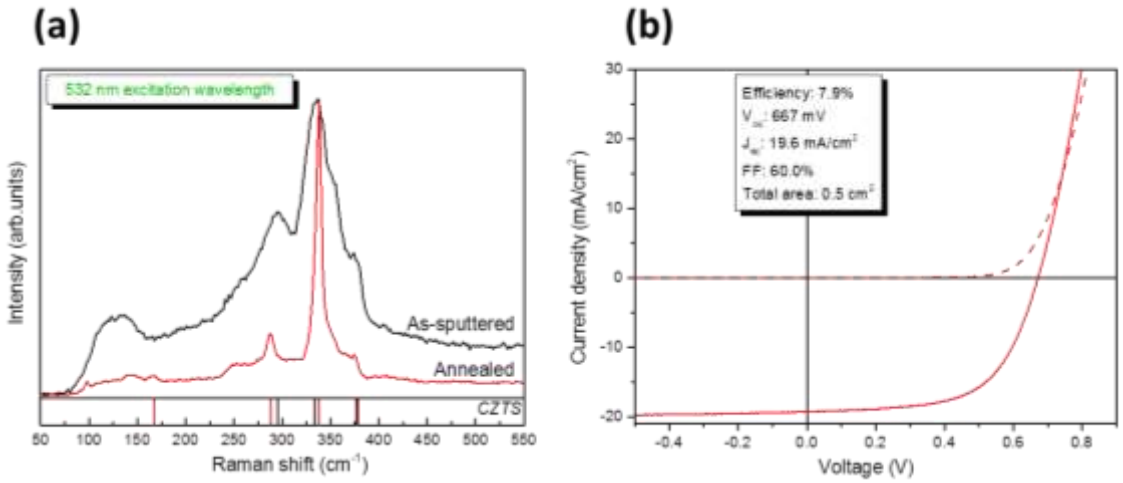

Figure 4 Raman spectra of typical as-sputtered and annealed films with 532 nm excitation wavelength (a) dark and illuminated J-V characteristics of the solar cell developed at UU-ASC, the standard structure of such device comprises of Al:ZnO/i-ZnO/CdS/CZTS/Mo/SLG, and the inset shows the device performance (b)

The standard CZTS solar cell structure contains Al:ZnO/i-ZnO/CdS/CZTS/Mo/SLG, and the device parameters are generally derived from the measured J-V curve, as plotted in Figure 1(b). The composition of high efficient CZTS devices from UU-ASC process is slightly Cu poor and Zn rich. The device in Figure 1(b) has 2000nm thick CZTS absorber. Our recent study on the influence of absorber thickness suggests that much further enhancement of the device performance can be achieved, if the buffer/CZTS interface and the absorber quality can be continuously improved.

The addition of Se via selenisation of the sulphide was implemented and resulted in a device efficiency of over 9 %. Figure 5 and table 2 show the results of recent developments in precursor development and their influence on of CZTS and CZTSSe device performance at UU_ASC.

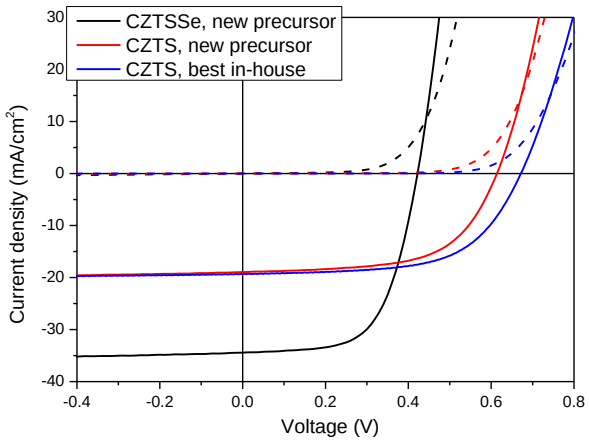

Figure 5: Light J-V curves for CZTS (the best achieved and the highest performance using new precursors) and CZTSSe devices produced at UU-ASC (details in table 2, below)

	V_{oc} [mV]	J_{sc} [mA/mc²]	FF [%]	PCE [%]	T. Area [cm²]
CZTS	667	19.6	60.0	7.9	0.5
CZTS, new	613	18.9	60.6	7.0	0.1
CZTSSe, new	421	34.4	62.0	9.0	0.5

Table 2: Light J-V parameters corresponding to the plots shown in Figure 5 (above) for CZTS (the best achieved and the highest performance using new precursors) and CZTSSe devices produced at UU-ASC.

In addition to the development of CZTS and CZTSSe absorber layers, research at UU-ASC has included the development of atomic layer deposition (ALD) and tuning of ZnSnO buffer layers to control V_{oc} values.

References

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Partner IREC

At IREC, a two-stage PVD process is used for the synthesis of high quality kesterite absorber material. This two-step process consists of deposition of Cu/Sn/Cu/Zn metallic precursor stacks onto Mo coated soda lime glass by DC sputtering followed by a selenization process in a conventional tube furnace using a graphite box and Se and Sn powder.[6]

Solar cells are fabricated from the p-type selenium pure kesterite (CZTSe) absorbers by employing a p-type absorber / n-type buffer/window heterostructure to form the pn-junction for the separation of light generated electron hole pairs as commonly used in thin film solar cell technology. The role of the buffer layer is to provide an optimal conduction band alignment of absorber/buffer/window heterostructure, which is crucial for high device performance. For kesterite absorbers highest device performances are achieved using CdS as buffer layer. An optimization of the CdS buffer layer performed in our group led to an increase of device performance up to 8.3% power conversion efficiency.[7 Furthermore, the surface near region of the CZTSe absorber is very crucial for the p-n junction formation with the buffer layer. Here, a

detailed study of the surface chemistry of selenium pure kesterite absorbers and it large influence on device performance helped to develop a post deposition low temperature annealing treatment that increase device efficiencies from below 3% to over 8%.[8] This low temperature post deposition annealing promotes a Cu-depletion and Zn enrichment of the CZTSe surface, which is mandatory for high device performance.

Further improvements in device performance could be achieved by developing a new innovative route of Ge assisted CZTSe synthesis.[9] This Ge-based approach is based on the evaporation of a 10 nm Ge layer on top of the Cu/Sn/Cu/Zn metallic precursor stack prior to the selenization process. Different to Ge substitution in CZTSe reported in literature so far [10], the small quantity employed in this approach still ensures the sustainability of the developed process because in the final synthesized CZTSe film only 1.6% of Sn is substituted by Ge. By employing this Ge based approach device performance could be increased to over 10.4% with remarkable high open circuit voltage (V_{oc}) vales up to 490 mV, which is the highest vale reported so far for CZTSe solar cells. Thus, the results are very promising to help to solve the high V_{oc} deficit, which is considered as one of the main challenges of this technology. The reasons for the improved device performance achieved by employing the Ge approach are currently under investigation.

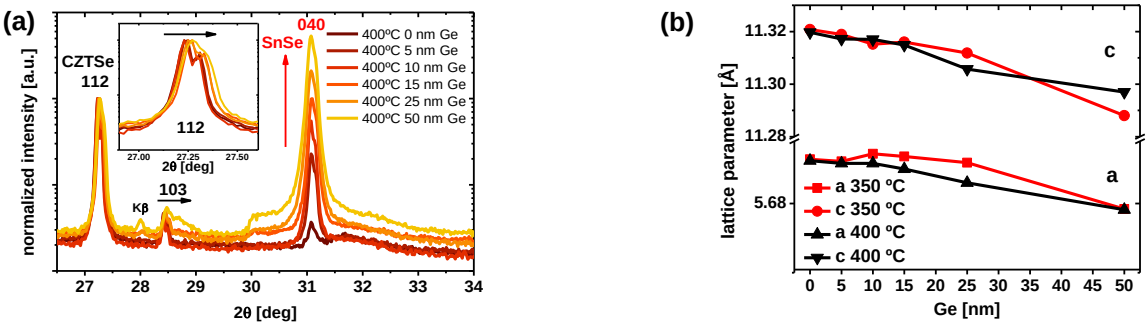

Figure 6, (a) Raman Spectra showing the influence of Ge-layer thickness on the peaks and measured SnSe of Ge-doped CZTSe and (b) the influence of Ge-layer thickness on lattice parameter.

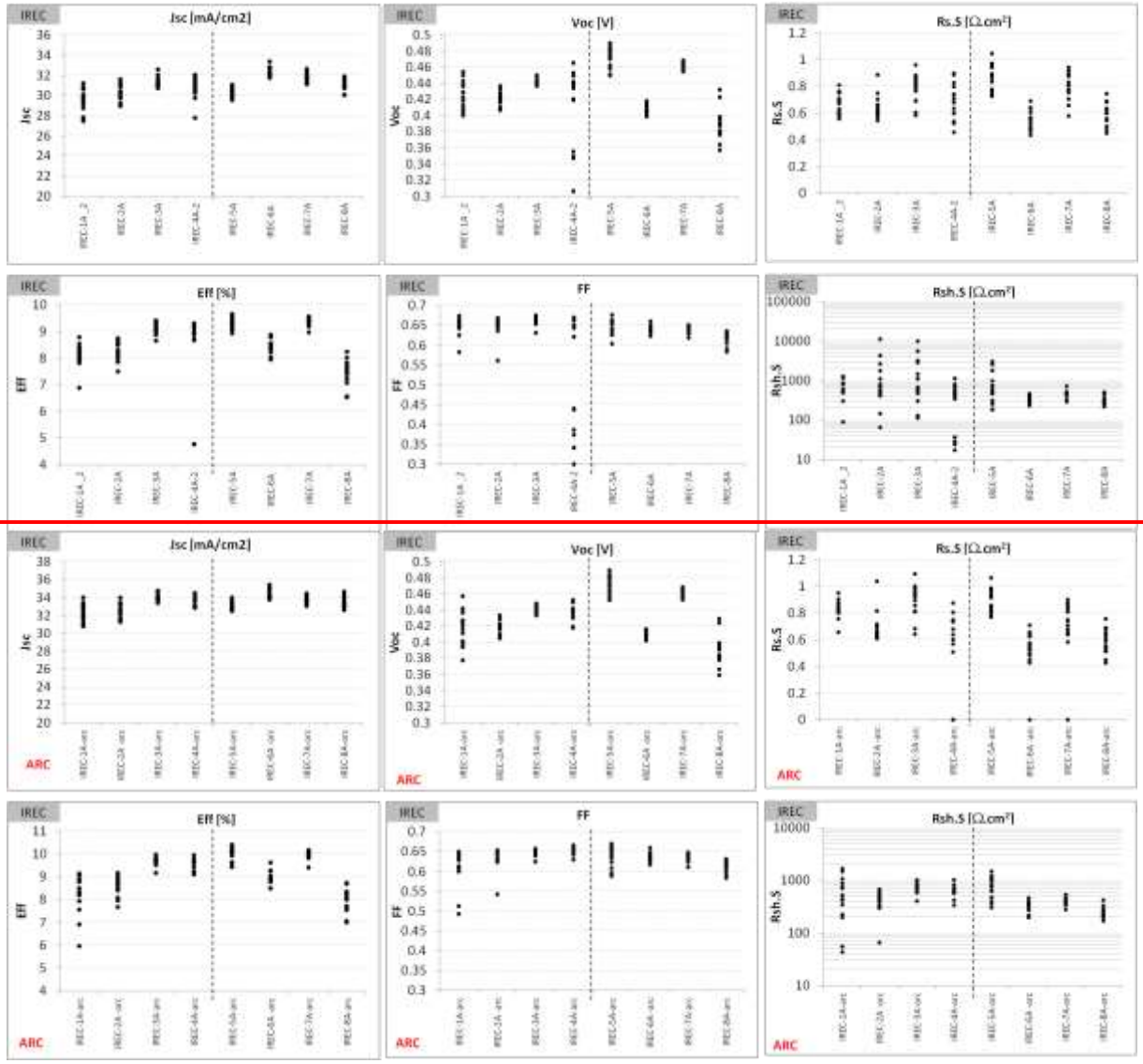

Figure 7 Optoelectronic parameters of CZTSe absorbers synthesized using a Ge based process. The upper part corresponds to cells without antireflective coating (ARC), and the lower part with ARC.

Best cell performance without ARC (average values in brackets):

Eff= 9.7% (8.4%), V_{oc} = 490mV (425mV), J_{sc} = 33.4 mA/cm^2 (30.9 mA/cm^2), FF= 67.6% (63.2%).

Best cell performance with ARC:

Eff= 10.4% (9.1%), V_{oc} = 489mV (430mV), J_{sc} = 35.4 mA/cm^2 (33.3 mA/cm^2), FF= 67.0% (63.3%)

In summary, at IREC a sequential route based in the deposition of metallic stacks and a subsequent reactive annealing under Se atmosphere has been developed. By the optimization of the absorber and the complete device, including back contact and CZTSe/CdS heterojunction, and with the inclusion of an innovative Ge-assisted synthesis[11], efficiencies up to 10.4% have been obtained (10.6% maximum not certified yet), with V_{OC} exceeding 490 mV, that represents the higher values reported at all for this absorber.

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Overall Summary

The work by the three partners within Work Package 2 has shown that PVD based processing based on the reactive annealing (or conversion) of sputtered precursor layers, are each capable of yielding device quality absorber layers. The material has the Kesterite structure with performances related to cation ratios as shown by NU and WP1. Conversion of mixed metal precursors (NU) or stacked 4-layer metal precursors (IREC) as well as annealing of reactively sputtered Cu_2ZnSnS_4 layers, yield device efficiencies above 8% and with the use of Ge-doping, over 10 %. However the main conclusions are that all-three synthesis routes have demonstrated that these have achieved, or are likely to achieve, the target conversion efficiency of 10%.

Although, the synthesis routes can be controlled, NU for instance, to produce near stoichiometric/single phase absorbers, currently the highest performance devices result from “non-stoichiometric” materials. The ability of each route to yield device quality Kesterite materials is critically dependent on the details of the deposition process and the subsequent conversion or annealing conditions. The non-vacuum process under investigation at IREC showed promise but progress for this route was terminated. However, the Non-vacuum process pursued in WP4 at EMPA also achieved a performance above 11 %. The overall conclusion is that whilst careful control of processing and composition is required. Device quality CZT(SSe) can be synthesised by both vacuum and non-vacuum routes and the processes material shows tolerance to variations in deposition and conversion technique. The work within WP2 has demonstrated and reinforced the key role that improvement of interfaces can make in increasing device performance.